

# APPROVAL SHEET

PRODUCT : LCD Module

MODEL NO : 20402

JE-AN ELECTRONICS CO.,LTD		
PREPARED	CHECKED	APPROVED

CUSTOMER		
PREPARED	CHECKED	APPROVED

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## 1. Features

- Display mode : STN / TN , Positive/Negative type display
- Display format : 20 Characters x 4 Lines
- Driving method : 1/16 Duty, 1/4 Bias
- Viewing direction : 6 O'clock/12 O'clock
- Back lighting : LED / EL unit

## 2. Mechanical Specifications

Item	Specification	Unit
Module Size (W x H x T)	146.0 x 62.5 x 13.1 Max.	mm
Viewing Area (W x H)	123.5 x 43.0	mm
Character Font (W x H)	5.0 x 7.0	dots
Character Size (W x H)	4.84 x 9.22	mm
Character Pitch (W x H)	6.0 x 9.75	mm
Dot Size (W x H)	0.92 x 1.1	mm
Weight	About 100	g

## 3. Electrical Specifications

### 3-1. Absolute Maximum ratings

Item	Symbol	Value			Unit	Condition	Remarks
		Min.	Typ.	Max.			
Supply Voltage	Logic	V <sub>DD</sub>	0	-	+7.0	V	T <sub>a</sub> = 25°C
	LCD	V <sub>DD-V0</sub>	0	-	V <sub>DD</sub> +0.3	V	T <sub>a</sub> = 25°C
Input voltage		V <sub>I</sub>	0	-	V <sub>DD</sub> +0.3	V	T <sub>a</sub> = 25°C
Operating temp.		T <sub>opr</sub>	-20	-	+70	°C	-
Storage temp.		T <sub>stg</sub>	-40	-	+85	°C	-

### 3-2. Electrical Characteristics

$V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ C \sim 50^\circ C$

Item		Symbol	Spec. Value			Unit	Condition
			Min.	Typ.	Max.		
Supply Voltage	Logic	$V_{DD}-V_{SS}$	4.5	5.0	5.5	V	-
	LCD	$V_{DD}-V_0$	-	5.0	-	V	$T_a = -30^\circ C$ $\Theta = 10^\circ$ , $\Phi = 0^\circ$
			4.5	4.7	5.5	V	$T_a = 25^\circ C$ $\Theta = 10^\circ$ , $\Phi = 0^\circ$
			-	4.4	-	V	$T_a = 85^\circ C$ $\Theta = 10^\circ$ , $\Phi = 0^\circ$
Supply Current	Logic	$I_{DD}$	-	0.5	2.0	mA	$V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$ $T_a = 25^\circ C$
	LCD	$I_0$	-	1.2	1.8	mA	
Power Consumption		$P_D$	-	500	-	mW	
Input Voltage "HIGH" Level		$V_{IH}$	2.2	-	$V_{DD}$	V	-
Input Voltage "LOW" Level		$V_{IL}$	-0.3	-	0.6	V	-
Output Voltage "HIGH" Level		$V_{OH}$	2.4	-	-	V	-
Output Voltage "LOW" Level		$V_{OL}$	-	-	0.4	V	-
Frame Frequency		$F_f$	-	84.3	-	Hz	$F_{osc} = 270KHz$
Oscillation Frequency		$F_{osc}$	125	270	350	Hz	$R_{osc} = 91k\Omega \pm 2\%$

## 4. Characteristics of Backlighting (LED Unit)

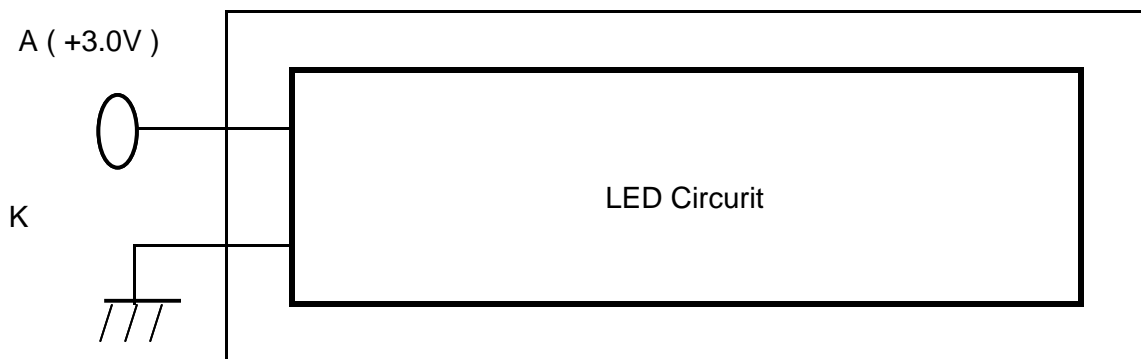
### 4-1. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit
Forward Current	$I_F$	$T_a = 25^\circ\text{C}$	-	200	mA
Reverse Voltage	$V_R$	$T_a = 25^\circ\text{C}$	-	5	V
Power Dissipation	$P_D$	$T_a = 25^\circ\text{C}$	-	2160	mW

### 4-2. Opto-electric Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	$V_F$	$T_a = 25^\circ\text{C}$	-	3.0	4.0	V
Luminous	-	$I_F = 200\text{mA}$	70	-	-	$\text{Cd}/\text{m}^2$

### 4-3. LED Circuit Diagram



## 5. Electro - Optical Characteristics

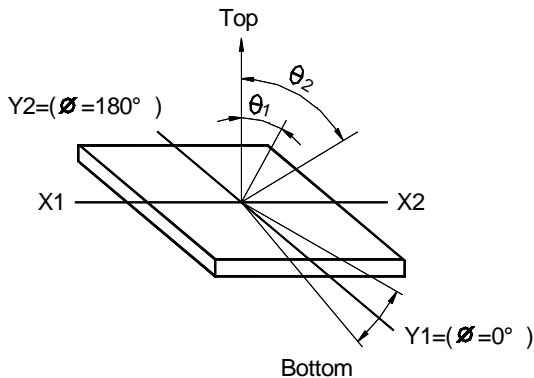
Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\Theta_2 - \Theta_1$	50	60	-	deg.	$Cr = 2$	1,2
	$\Phi$	$\pm 35$		-			
Contrast Ratio	Cr	3	5	-	-	$\Theta = 10^\circ$ $\Theta = 0^\circ$	3
Response Time (rise)	Tr	-	150	250	ms	$\Theta = 10^\circ$ $\Theta = 0^\circ$	4
Response Time (full)	Tf	-	150	250	ms	$\Theta = 10^\circ$ $\Theta = 0^\circ$	4

● Above data are measured under 1/16 Duty STN Gray mode

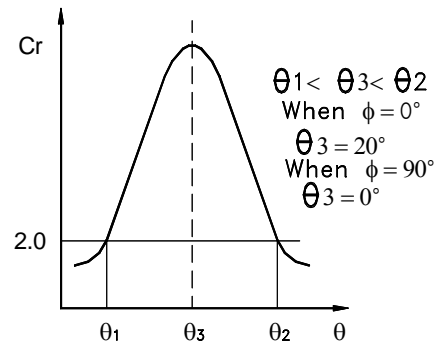
Ta= 25.°

●  $\Theta = 0$  means viewing direction

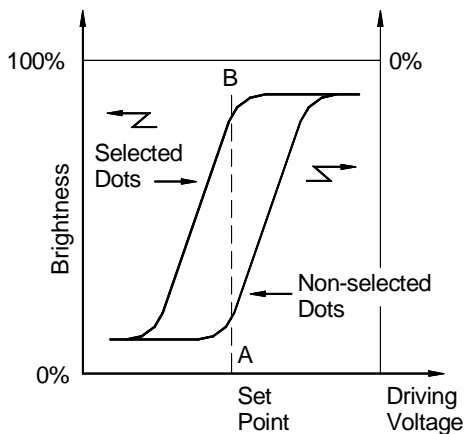
Note 1. Definition of angle  $\theta$  and  $\phi$



Note 2. Definition of viewing angle  $\theta_1$  and  $\theta_2$

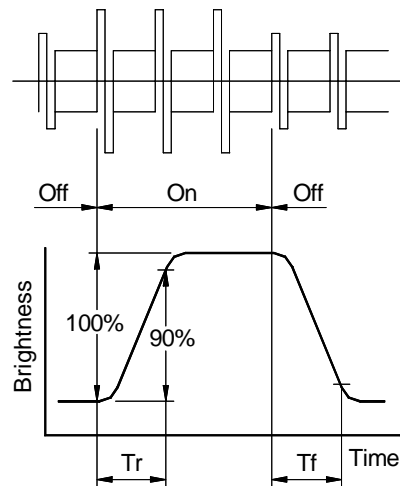


Note 3. Definition of contrast Cr



$$Cr = (A/B)^P \begin{cases} \text{Negative : } P = -1 \\ \text{Positive : } P = +1 \end{cases}$$

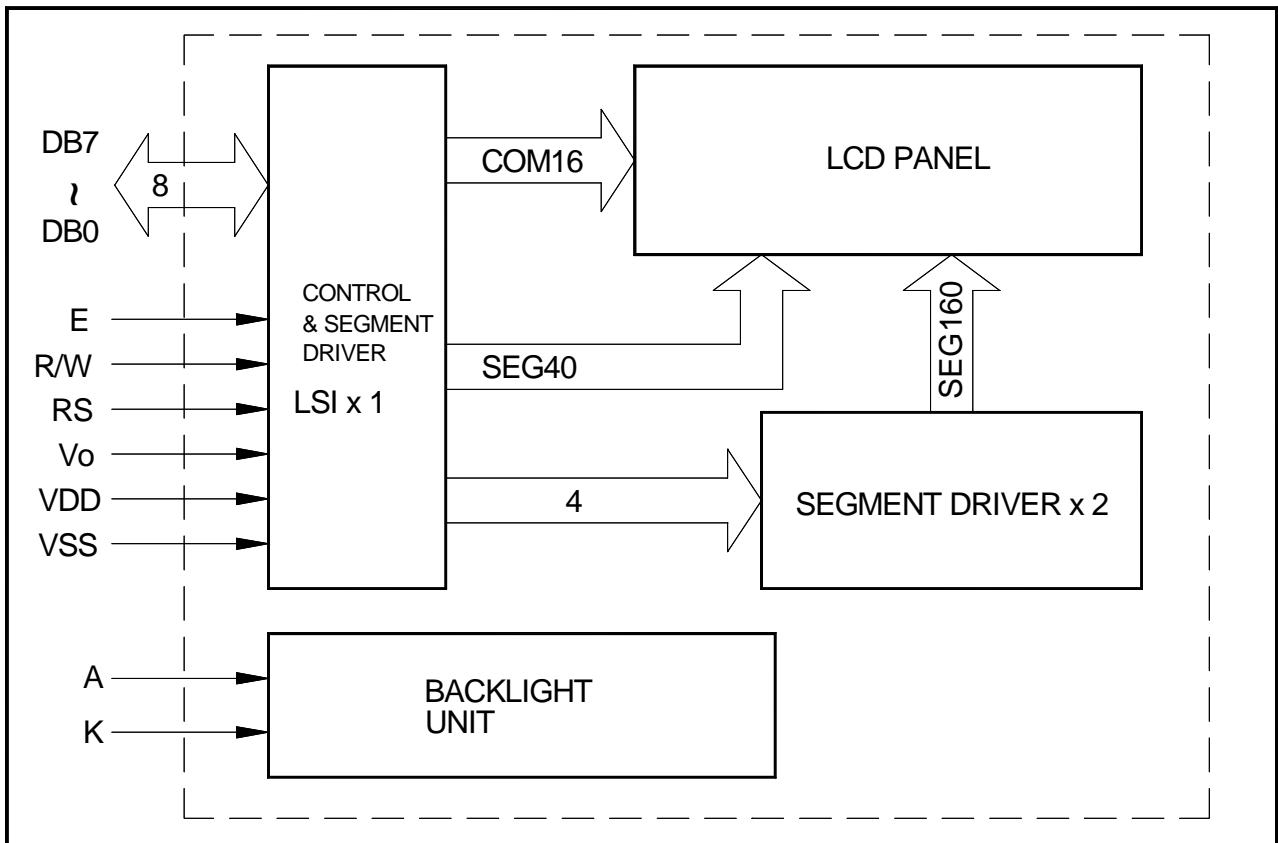
Note 4. Definition of optical response



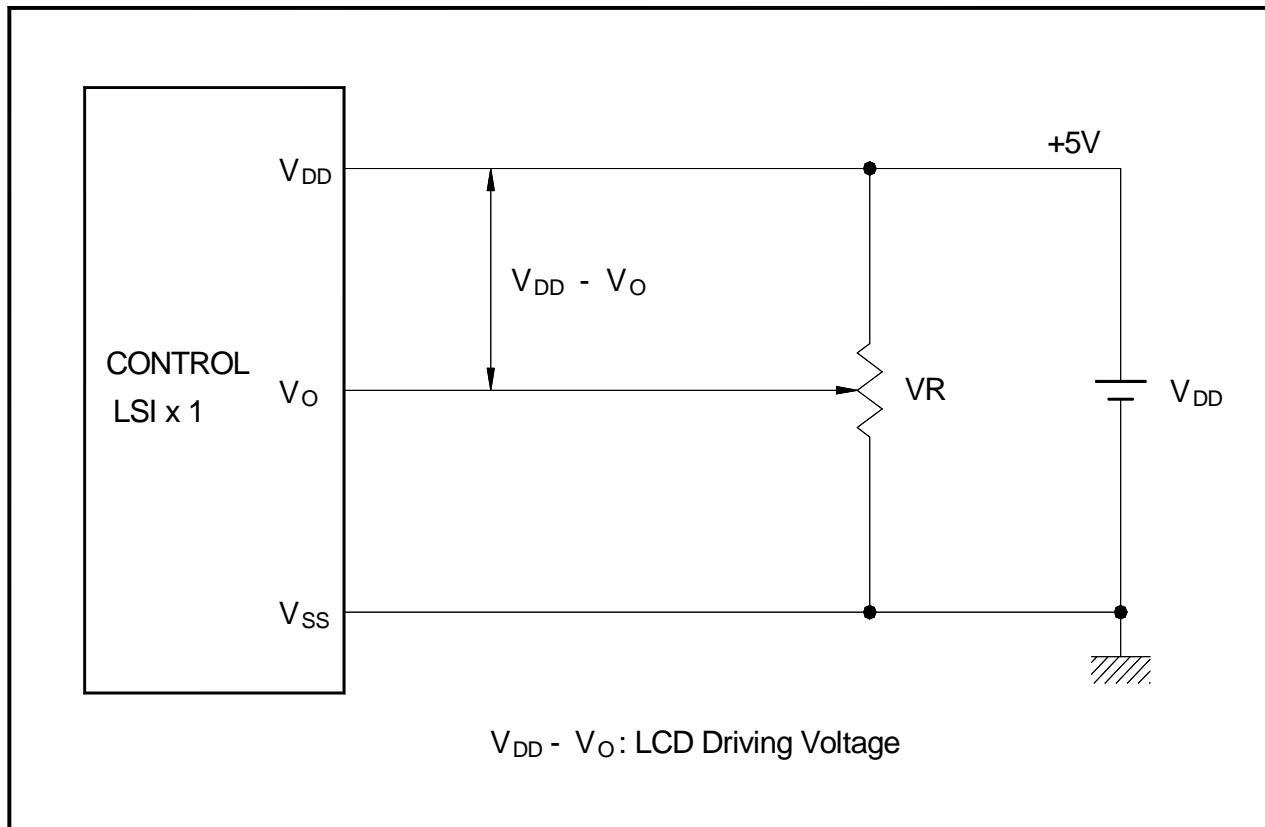
## 6. Pin Assignment

Pin No.	Symbol	Level	Function
1	V <sub>SS</sub> (GND)	0 V	Ground
2	V <sub>DD</sub> (V <sub>CC</sub> )	+ 5V	Logic Supply Voltage
3	V <sub>0</sub>	-	LCD Driving Voltage
4	RS	H / L	H : Data Input L : Instruction Input
5	R / W	H / L	H : Data Read L : Data Write
6	E	H, H → L	Enable Signal
7	DB0	H / L	Data Bus Line
8	DB1	H / L	
9	DB2	H / L	
10	DB3	H / L	
11	DB4	H / L	
12	DB5	H / L	
13	DB6	H / L	
14	DB7	H / L	
15	A	LED (+)	Power Supply ofr LED
16	K	LED (-)	
17	NC	-	
18	NC	-	

## 7. Block Diagram



## 8. Power Supply Block Diagram



## 9. Timing Characteristics

$V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = -30^\circ C \sim +85^\circ C$

Item	Symbol	Value			Unit	
		Min.	Typ.	Max.		
Enable Cycle Time	Fig 1, 2	$T_{CYC}$	500	-	-	ns
Enable Pulse Width, High Level	Fig 1, 2	$PW_{EH}$	230	-	-	ns
Enable Rise and Fall Time	Fig 1, 2	$t_{ER}, t_{EF}$	-	-	25	ns
Address Setup Time, RS, R/w, E	Fig 1, 2	$T_{AS}$	40	-	-	ns
Data Delay Time	Fig 2	$T_D$	-	-	120	ns
Data Setup Time	Fig 1	$T_{DSW}$	80	-	-	ns
Data Hold Time	Fig 1	$T_H$	10	-	-	ns
Data Hold Time	Fig 2	$T_{DH}$	20	-	-	ns
Address Hold Time	Fig 1, 2	$T_{AH}$	10	-	-	ns

FIG.1 Write Operation (MPU -> LCD MODULE)

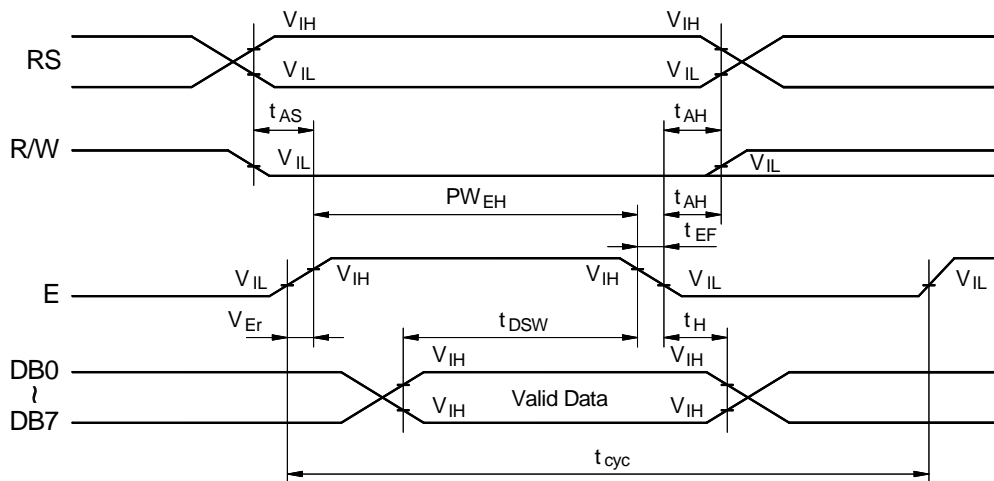
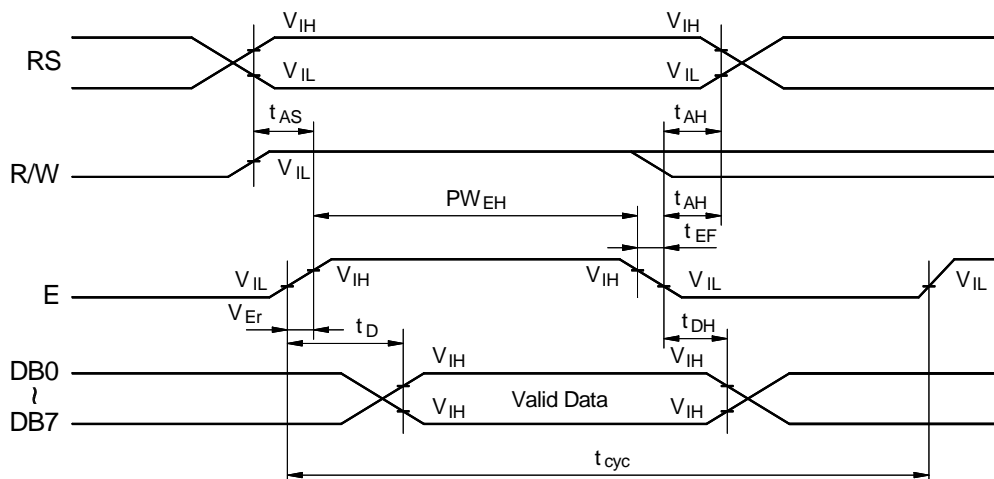


FIG.2 Read Operation (LCD MODULE -> MPU)



# 10. Instruction Sets

## 10-1. Instruction

Instruction	Code										Description	Execution Time(Max) Fosc is 270KHz	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	1		1.52 ms	
Return Home	0	0	0	0	0	0	0	0	0	1	*	Returns display being shifed	1.52 ms
Entry mode Set	0	0	0	0	0	0	0	0	1	I/D	SH		37 $\mu$ s
Display On/Off Cotrol	0	0	0	0	0	0	0	1	D	C	B		37 $\mu$ s
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	*	*		37 $\mu$ s
Function Set	0	0	0	0	0	1	DL	N	F	*	*		37 $\mu$ s
Set CG Ram Address	0	0	0	1	ACG							37 $\mu$ s	
Set DD Ram Address	0	0	1	ADD							37 $\mu$ s		
Read Busy Flag and Address	0	1	BF	ADD							0 $\mu$ s		
Write Data to CG or DD Ram	1	0	AC							43 $\mu$ s			
Read Data From CG or DD Ram	1	1	Read							43 $\mu$ s			

Remarks				
I/D	1	Increment	0	Decrement
SH	1	Entire Shift on	0	Entire Shift off
S/C	1	Display Shift	0	Cursor move
R/L	1	Shift to the Right	0	Shift to the Left
DL	1	8 Bits	0	4 Bits
N	1	2 Lines	0	1 Lines
F	1	5 x 11 Dots	0	5 x 8 Dots
BF	1	Internally Operating	0	Can accept instruction

DD RAM : Display Data RAM

CG RAM : Character Generator RAM

ACG : CG RAM Address

ADD : CG RAM Address : Corresponds to cursor Address

AC : Address counter used for both

DD and CG RAM Address

● : No Effect ( Don't Care )

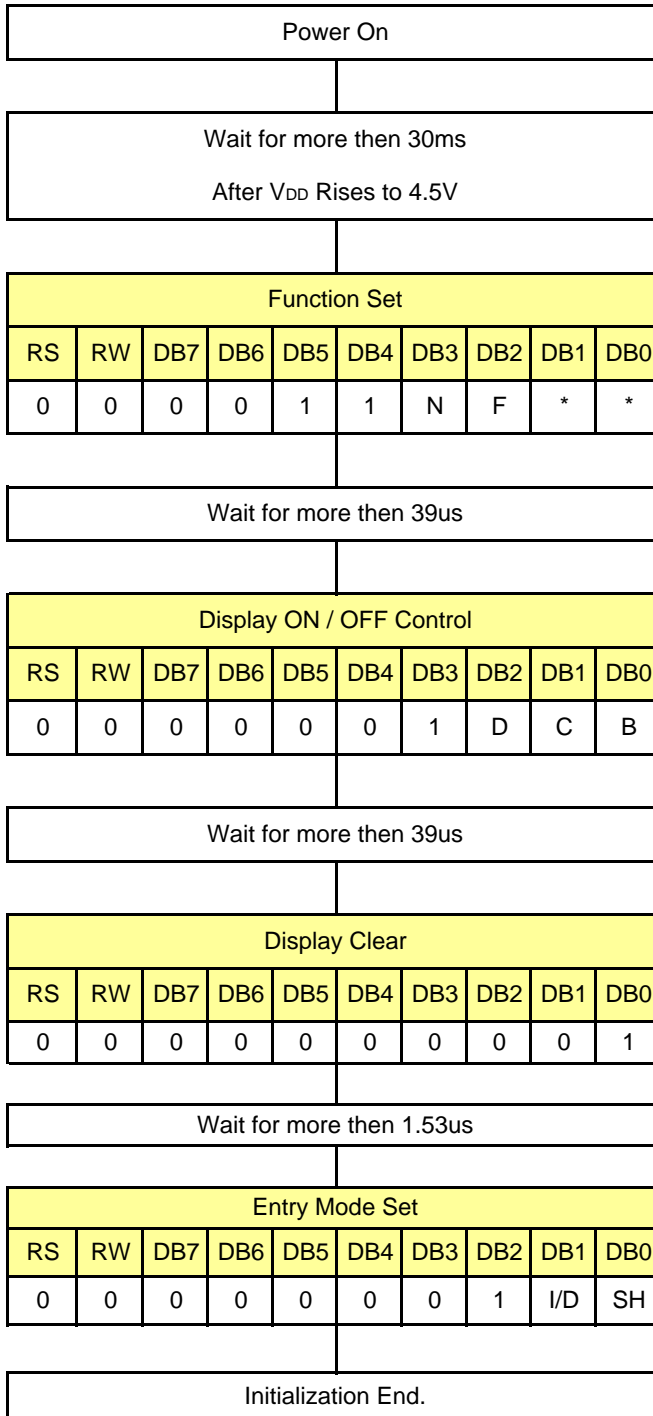
## 10-2. Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, Initialization by instruction is required.

Use the Following procedure for initialization.

### 10-2-1. When Interface Is 8 Bits Long :

Condition : fosc = 270KHz



Display Off

Display Clear

Entry Mode Set

N	0	1-Line Mode.
	1	2-Line Mode.
F	0	Display off
	1	Display on

D	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
B	0	Blink off
	1	Blink on

I/D	0	Decrement mode
	1	Increment mode
SH	0	Entire shift off
	1	Entire shift on

## 9-2-2. When interface is 4 Bits Long : Condition : fosc = 270KHz

Power On

Wait for more then 30ms  
After VDD Rises to 4.5V

Function Set					
RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	1	0
0	0	0	0	1	0
0	0	N	F	*	*

Wait for more then 39us

Display ON / OFF Control					
RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	1	D	C	B

Wait for more then 39us

Display Clear					
RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	0	0	0	1

Entry Mode Set					
RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	0	1	I/D	SH

Initialization Ends.

Display Off

Display Clear

Entry Mode Set

N	0	1-Line mode
	1	2-Line mode
F	0	Display off
	1	Display on

D	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
B	0	Blink off
	1	Blink on

I/D	0	Decrement mode
	1	Increment mode
SH	0	Entire shift off
	1	Entire shift on

## 9-3. DD RAM Address

Digit	1	2	3	4	5	6	7	8	----	----	15	16	17	18	19	20
1-Line	00	01	02	03	04	05	06	07	----	----	0E	0F	10	11	12	13
2-Line	40	41	42	43	44	45	46	47	----	----	4E	4F	50	51	52	53
3-Line	14	15	16	17	18	19	1A	1B	----	----	22	23	24	25	26	27
4-Line	54	55	56	57	58	59	5A	5B	----	----	62	63	64	65	66	67

Display position  
DD RAM Address  
( Hexadecimal )

# 11. Character Font Table

Upper 4bit Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HLLL	(7)															
HHHH	(8)															

